

Application Serial No. 09/407,204
Examiner: N. Parekh
Art Unit: 2811

PATENT
M&G No. 08688.0128US01

In the Claims

Please amend the claims as follows. No new matter has been added.

1. (Currently Amended) A semiconductor chip module comprising:

a chip-mounting member having opposite first and second surfaces, a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;

a first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a first dielectric tape member for bonding adhesively said first semiconductor chip on said chip-mounting member;

a first conductor unit for connecting electrically said contact pads of said first semiconductor chip and said first circuit traces; and

a plurality of solder balls disposed on one of said first and second surfaces of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member;

wherein said first circuit traces and said first semiconductor chip are disposed on a same one of said first and second surfaces of said chip-mounting member;

said first dielectric tape member bonds adhesively said pad mounting surface of said first semiconductor chip on said same one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said first semiconductor chip; and

said first conductor unit includes a plurality of conductive contact balls that are ~~received~~ disposed within said holes in said first dielectric tape member to establish electrical connection between said contact pads of said first semiconductor chip and said first circuit traces.

Claim 2 (canceled)

Application Serial No. 09/407,204
Examiner: N. Parekh
Art Unit: 2811

PATENT
M&G No. 08688.0128US01

3. (Currently Amended) The semiconductor chip module as claimed in Claim 2 1, wherein said chip-mounting member further has a set of second circuit traces accessible from the other one of said first and second surfaces opposite to said first circuit and connected to said plated through holes, said semiconductor chip module further comprising:

a second semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a second dielectric tape member for bonding adhesively said second semiconductor chip on said chip-mounting member; and

a second conductor unit for connecting electrically said contact pads of said second semiconductor chip and said second circuit traces.

4. (Original) The semiconductor chip module as claimed in Claim 3, wherein:

said second dielectric tape member bonds adhesively said pad mounting surface of said second semiconductor chip on the other one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said second semiconductor; and

said second conductor unit includes a plurality of conductive contact balls that are received in said holes in said second dielectric tape member to establish electrical connection between said contact pads of said second semiconductor and said second circuit traces.

5. (Currently Amended) The semiconductor chip module as claimed in Claim 2 1, wherein said first semiconductor has a peripheral portion that is provided with an epoxy resin layer to strengthen bonding of said first semiconductor chip with said same one of said first and second surfaces of said chip-mounting member.

6. (Currently Amended) The semiconductor chip module as claimed in Claim 2 1, wherein said first semiconductor chip has a heat dissipating surface that is opposite to said pad mounting surface and that has a heat dissipating plate secured thereon.

Application Serial No. 09/407,204
Examiner: N. Parekh
Art Unit: 2811

PATENT
M&G No. 08688.0128US01

Claims 7-18 (canceled)

19. (Currently Amended) A semiconductor chip module stack, comprising:

upper and lower semiconductor chip modules, each including

a chip-mounting member having upper and lower surfaces, a set of circuit traces, and a plurality of plated through holes that extend through said upper and lower surfaces and that are connected to said circuit traces,

a semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon,

a dielectric tape member for bonding adhesively said semiconductor chip on said chip-mounting member,

a conductor unit for connecting electrically said contact pads of said semiconductor chip and said circuit traces, and

a plurality of solder balls disposed on said lower surface of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member,

wherein said circuit traces and said semiconductor chip are disposed on a same one of said upper and lower surfaces of said chip-mounting member;

said dielectric tape member bonds adhesively said pad mounting surface of said semiconductor chip on said same one of said upper and lower surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said semiconductor chip;

said conductor unit includes a plurality of conductive contact balls that are ~~received in~~ disposed within said holes in said dielectric tape member to establish electrical connection between said contact pads of said semiconductor chip and said circuit traces; and

said solder balls of said upper semiconductor chip module are aligned with and are connected to said plated through holes in said chip-mounting member of said lower semiconductor chip module at said upper surface of said chip-mounting member of said lower semiconductor chip module.

Application Serial No. 09/407,204
Examiner: N. Parekh
Art Unit: 2811

PATENT
M&G No. 08688.0128US01

20. (Currently Amended) A semiconductor chip module comprising:

a chip-mounting member having opposite first and second surfaces, a set of first circuit traces, a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces, and a set of second circuit traces accessible from the other one of said first and second surfaces opposite to said first circuit traces and connected to said plated through holes;

a first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a first dielectric tape member for bonding adhesively said first semiconductor chip on said chip-mounting member;

a first conductor unit for connecting electrically said contact pads of said first semiconductor chip and said first circuit traces;

a second semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a second dielectric tape member for bonding adhesively said second semiconductor chip on said chip-mounting member;

a second conductor unit for connecting electrically said contact pads of said second semiconductor chip and said second circuit traces; and

a plurality of solder balls disposed on one of said first and second surfaces of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member;

wherein:

said first circuit traces and said first semiconductor chip are disposed on a same one of said first and second surfaces of said chip-mounting member;

said first dielectric tape member bonds adhesively said pad mounting surface of said first semiconductor chip on said same one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said first semiconductor chip;

Application Serial No. 09/407,204
Examiner: N. Parekh
Art Unit: 2811

PATENT
M&G No. 08688.0128US01

said first conductor unit includes a plurality of conductive contact balls that are ~~received~~ disposed within said holes in said first dielectric tape member to ~~establish~~ establish electrical connection between said contact pads of said first semiconductor chip and said first circuit traces;

said second dielectric tape member bonds adhesively said pad mounting surface of said second semiconductor chip on the other one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said second semiconductor chip; and

said second conductor unit includes a plurality of conductive contact balls that are ~~received in~~ disposed within said holes in said second dielectric tape member to establish electrical connection between said contact pads of said second semiconductor chip and said second circuit traces.

21. (Previously Added) The semiconductor chip module as claimed in claim 20, wherein each of said solder balls being connected to one of said first and second circuit traces.